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APPLICATION

FOR

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TITLE: **RC NETLIST REDUCTION FOR TIMING AND NOISE ANALYSIS**

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RC NETLIST REDUCTION FOR TIMING AND NOISE ANALYSIS

Background of Invention

[0001] The capabilities of modern integrated circuits ("ICs") continue to increase as technology improves. In order to increase the capabilities of an IC without increasing the size of the IC, sizes of devices on the IC must often be reduced to units of microns (10^{-6}). Circuit designs using devices having sizes measurable in microns are known and referred to as deep submicron ("DSM") designs.

[0002] A typical IC having a DSM design has tens of millions of devices. With this increased number of devices, there are more devices per unit area than a non-DSM design IC. To connect the devices to the IC substrate itself and with other circuit devices and components, physical wires, known as interconnect, form a network of connections on the IC. From a technical viewpoint, interconnect does not behave as a virtual or ideal wire. Instead, the interconnect acts similarly to a network of capacitances and resistors, which can dominate circuit behavior, particularly with regard to timing. Figure 1 shows a section of interconnect (10) on a typical IC (12). The interconnect (10) have inherent resistances (not shown) and capacitances (14). The section of interconnect (10) shown in Figure 1 is typically part of a larger network of interconnect known and referred to as a "RC network."

[0003] As the number of interconnect in a RC network increase with more devices per unit area on a DSM design IC, device performance, e.g., timing, signal integrity, power problems, etc., coupled with the demands for increased reliability, speed, and efficiency becomes increasingly harder to manage. In order to meet such demands, chip designers use automated tools to verify physical design and ensure circuit integrity.

[0004] One method used to facilitate the analysis and testing of an IC's interconnect is parasitic extraction. Parasitic extraction is the process of creating an electrical model representation of the physical connections present between devices in an IC. The electrical model formed as a result of parasitic extraction is typically known and referred to as a "netlist."

[0005] Reduction entails removing unintentional circuit elements to ensure circuit integrity. One goal of typical reduction techniques is to make a netlist as compact as possible while preserving accuracy as much as possible.

[0006] Figures 2a and 2b respectively show an original circuit (20) before a typical reduction process and a reduced circuit (30) after the typical reduction process. As shown in Figure 2b, a topology of the reduced circuit (30) is different from a topology of the original circuit (20). Further, the reduced circuit (30) has resistive loops (32) that were not present in the original circuit (20). Further still, the reduced circuit (30) has ground resistances (34) that were not present in the original circuit (20).

[0007] In effect, the typical reduction process results in a netlist that is topologically and functionally different from an original circuit. In addition, with a typical reduction process, because modern circuits have large numbers of input/output ports, there is a tendency for the reduction process to couple input/output ports with each other; thereby actually increasing the size of the circuit. Thus, there is a need for a reduction process that maintains an original circuit's topology while maintaining functional accuracy in a netlist with respect to the function and characteristics of the original circuit.

Summary of Invention

[0008] According to one aspect of the present invention, a circuit reduction method comprises inputting information about an original circuit structure, using a

resistive degree of at least one node in the original circuit structure to selectively sort the at least one node, determining at least one time constant of the original circuit, sorting the at least one time constant, and determining whether to remove a loop in the original circuit structure based on the sorted at least one time constant and the sorted at least one node.

[0009] According to another aspect, a computer-readable medium having recorded therein instructions executable by processing, where the instructions are for: inputting information about an original circuit structure; using a resistive degree of at least one node in the original circuit structure to selectively sort the at least one node; determining at least one time constant of the original circuit; sorting the at least one time constant; and determining whether to remove a loop in the original circuit structure based on the sorted at least one time constant and the sorted at least one node.

[0010] According to another aspect, a computer system comprises a processor, a memory, and instructions that reside in the memory and are executable by the processor, where the instructions are for: inputting information about an original circuit structure; using a resistive degree of at least one node in the original circuit structure to selectively sort the at least one node; determining at least one time constant of the original circuit; sorting the at least one time constant; and determining whether to remove a loop in the original circuit structure based on the sorted at least one time constant and the sorted at least one node.

[0011] Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

Brief Description of Drawings

[0012] Figure 1 shows a network of interconnects on a typical computer chip.

[0013] Figures 2a and 2b respectively show a circuit before and after a typical

reduction process.

[0014] Figure 3 shows a flow process in accordance with an embodiment of the present invention.

[0015] Figure 4a shows a circuit for a reduction process in accordance with an embodiment of the present invention.

[0016] Figure 4b shows a circuit reduction process in accordance with an embodiment of the present invention.

[0017] Figures 5a-5c show a circuit reduction process in accordance with another embodiment of the present invention.

Detailed Description

[0018] Embodiments of the present invention relate to a method and apparatus for generating a netlist that maintains a topology of an original circuit while preserving an original circuit's functions and characteristics. Embodiments of the present invention further relate to a method and apparatus for reducing a circuit using a process that maintains both (1) an original circuit topology and (2) functional characteristics of the original circuit.

[0019] Figure 3 shows an exemplary flow process in accordance with an embodiment of the present invention. Initially, a detailed standard parasitic format ("DSPF) is read (step 40). The DSPF has information regarding a structure of an original circuit. Once the DSPF has been read (step 40), a preprocessing phase occurs (step 42). The preprocessing phase involves preparing the original circuit such that it can be reduced. Thereafter, one or more nodes of the original circuit are sorted based on resistive degrees of the one or more modes (step 44).

[0020] Then, a timer is used to measure one or more time constants of the original circuit (step 46). Once the time constants have been determined (step 46), the time

constants are evaluated and sorted (step 48). Using the evaluated and sorted time constant information, one or nodes in the original circuit are analyzed (step 50) in order to determine which loops of the original circuit to eliminate (step 52). Once one or more loops are eliminated from the original circuit, a time measurement may again be made (step 46) to determine one or more time constants of the modified circuit. After the loops are removed (step 54), a reduced circuit results, where after, the reduced circuit is post-processed and stored in a new DSPF file (step 56).

[0021] Figures 4a shows a circuit for a reduction process in accordance with an embodiment of the present invention. Particularly, Figure 4a shows a model of a node. In the reduction process, resistances and ground capacitances are redistributed by eliminating nodes with insignificant characteristic time constants based on local circuit transformation in order to keep an Elmore time constant from all directions. The characteristic time constant of a node is defined as:

$$\tau_C = \chi / \gamma = \Sigma C / \Sigma g, \tag{1}$$

where $\chi = \Sigma C$ represents the total capacitance (including C_c and C_g) connected to a central node, and $\gamma = \Sigma g$ represents the total conductance connected to the central node. Further, τ_C is a measure of the significance of a node.

[0022] Those skilled in the art will appreciate that the elimination of insignificant nodes, there is only a relatively small effect in the time domain response. The critical time constant is determined by using a built-in fast delay and noise estimation engine to control the reduction process.

[0023] Still referring to Figure 4a, if R_{iN} and R_{jN} are present, then connect node *i* and node *j* with R_{ij}, where $R_{ij} = \gamma_N / (g_{iN} * g_{jN})$. If R_{iN} and C_{jN} are present, then connect node *i* and node *j* with C_{ij}, where $C_{ij} = (g_{iN} * C_{jN}) / \gamma_N$.

[0024] Figure 4b shows an exemplary circuit reduction process in accordance with

an embodiment of the present invention. Particularly, the reduction process shows the steps in a circuit transformation according to values for R_{iN}, R_{jN}, γ_N, and C_{ij}.

[0025] Figure 5a-5c show an original circuit, a circuit reduced using traditional means, and a circuit reduced in accordance with embodiments of the present invention.

[0026] Those skilled in the art will appreciate that a circuit reduction method in accordance with embodiments of the present invention maintain global ground capacitance distribution along a particular net. Further, those skilled in the art will appreciate that the circuit reduction method maintains the global coupling capacitance distribution along a particular net. Those skilled in the art will also appreciate that the circuit reduction method maintains spatial latency, i.e., the coupling between a near end node and a far end node.

[0027] Additionally, those skilled in the art will appreciate that a reduction tool related to the present invention allows a user to select a node for reduction.

[0028] Furthermore, those skilled in the art will appreciate that a reduction tool related to the present invention reduces an original circuit regardless of the number of input/output ports in the original circuit. Thus, unlike the typical reduction tool, the present invention compensates for input/output port linkages and ensures actual reduction, i.e., an actual decrease in circuit size.

[0029] Advantages of the present invention may include one or more of the following. In some embodiments, a reduced circuit may be generated that has a similar topology of an original circuit.

[0030] In some embodiments, because a circuit reduction method maintains coupling capacitance distribution along a net, accuracy is increased relative to when the coupling capacitance distribution along the net is not uniform.

[0031] In some embodiments, a reduced circuit may be generated that maintains

the total ground capacitance present in an original circuit.

[0032] In some embodiments, a reduced circuit may be generated that maintains the total resistance of an original circuit.

[0033] In some embodiments, a reduced circuit may be generated that removes loops present in an original circuit.

[0034] In some embodiments, a circuit reduction tool reduces a size of an original circuit regardless of the amount and positions of input/output ports in the original circuit.

[0035] In some embodiments, a circuit reduction method has error control by which a user may specify an amount of error that can be tolerated in the circuit reduction method.

[0036] In some embodiments, a circuit reduction tool is able to remove loops that are not present in an original circuit structure but are present after a reduction extraction of the original circuit.

[0037] In some embodiments, a circuit reduction tool allows a user to select which nodes to reduce.

[0038] While the invention has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be devised which do not depart from the scope of the invention as disclosed herein. Accordingly, the scope of the invention should be limited only by the attached claims.